

Response Under 37 C.F.R. §1.116  
Expedited Procedure  
Examining Group 2811

### **REMARKS**

#### **Response to the §103 Rejections of Claims 1-4, 6-9, 12-14 and 17-19**

In the June 8, 2006 Final Office Action, the Examiner rejected claims 1-4, 6-9, 12-14 and 17-19 under 35 U.S.C. §103(a) as alleged obvious over the combinations of various references. Specifically, the Examiner rejected:

- Claims 1, 6-9, 12-14 and 17-19 under 35 U.S.C. §103(a) as alleged obvious over the combination of U.S. Patent No. 6,063,681 to Son (hereinafter "Son") and U.S. Patent No. 6,051,494 to Iwamatsu et al. (hereinafter "Iwamatsu");
- Claims 2-3 under 35 U.S.C. §103(a) as alleged obvious over the combination of Son and Iwamatsu further in view of U.S. Patent No. 6,313,020 to Kim et al. (hereinafter "Kim"); and
- Claim 4 under 35 U.S.C. §103(a) as alleged obvious over the combination of Son and Iwamatsu further in view of U.S. Patent No. 6,399,452 to Krishnan et al. (hereinafter "Krishnan").

In response, Applicants have hereby amended the independent claim 1, from which claims 2-4, 6-9, 12-14, and 17-19 depend, to positively recite a method for forming a low resistance MOSFET device by sequentially forming: (1) the gate region, (2) the source/drain extension regions and the channel region, (3) the first spacers, (4) the source and drain regions, (5) the first silicide regions, (6) the second spacers, and (7) the second silicide regions.

Support for such claim amendments can be found in FIGS. 3a-3h of the instant specification and related descriptions thereof. Specifically, FIG. 3a shows formation of a gate region 5 atop a surface of a substrate 10; FIG. 3b shows subsequent formation of source and drain extension regions 7 in the substrate 10, while a channel region 9 is formed between the source and drain extension regions 7 in the substrate 10; FIG. 3c shows subsequent formation of first spacers 14; FIG. 3d shows subsequent formation of source and drain regions 6; FIG. 3f shows subsequent formation of first silicide regions 11; FIG. 3g shows subsequent formation of second spacers 15; and FIG. 3h shows subsequent formation of second silicide regions 12.

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It is important to note the claimed method of the present invention not only forms the recited MOSFET components, but also forms such MOSFET components according to a specific sequential order, as positively recited by claims 1-4, 6-9, 12-14, and 17-19 of the present application.

None of the cited references teaches or suggests formation of the recited MOSFET components at such a specific sequential order.

Specifically, the Son reference teaches various methods for forming similar MOSFET components, but at significantly different sequential orders (see Son, FIGS. 3A-5G).

The secondary references Iwamatsu, Kim, and Krishnan do not even teach formation of all of the recited MOSFET components, much less at the specific sequential order as recited by claims 1-4, 6-9, 12-14, and 17-19 of the present application, and therefore cannot remedy the deficiency of Son.

Therefore, claims 1-4, 6-9, 12-14, and 17-19 of the present application patentably distinguish over the cited references, by positively recite a method for forming a low resistance MOSFET device by sequentially forming: (1) the gate region, (2) the source/drain extension regions and the channel region, (3) the first spacers, (4) the source and drain regions, (5) the first silicide regions, (6) the second spacers, and (7) the second silicide regions.

Based on the foregoing, claims 1-4, 6-9, 12-14, and 17-19 as amended herein are in condition for allowance. Issue of a Notice of Allowance for the application is therefore requested.

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Examining Group 2811

If any issues remain outstanding, incident to the formal allowance of the application, the Examiner is requested to contact the undersigned attorney at (516) 742-4343 to discuss same, in order that this application may be allowed and passed to issue at an early date.

Respectfully submitted,



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